REMARKS

This paper is responsive to the Final Office action dated July 28, 2005. Claims 1-7, 9-14, 16-21, 24, 26, 27 and 31-33 were examined. Applicant notes that a Notice of Appeal is being submitted herewith to potentially avoid additional extension fees. The Examiner is respectfully requested to contact the undersigned at the Examiner's convenience to discuss the claims.

Claim Rejections – 35 USC § 112

Claims 26-27 and 31-33 stand rejected under 35 U.S.C. § 112, first and second paragraphs.

Claim Rejections – 35 USC § 102

Claims 1-7, 9, 14, 19-20, 26, and 31-32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Baweja et al., U.S. Patent No. 6,212,599 (hereinafter "Baweja).

Claim Rejections – 35 USC § 103

Claim 27 stands rejected under 35 U.S.C. § 103(a) as being unpatentable under Baweja in view of Henkhaus et al., U.S. Patent No. 6,654,895 (hereinafter "Henkhaus").

Claim 33 stands rejected under 35 U.S.C. § 103(a) as being unpatentable under Baweja.

Allowed and Allowable Subject Matter

Applicant appreciates the indication that claims 21 and 24 are allowed and that claims 10-13 and 16-18 are indicated as containing allowable subject matter, which would be allowable if rewritten in independent form.

Applicant's Arguments

Claims 1, 9, and 14

Claim 1 was amended to incorporate the subject matter of claim 13, which was indicated as allowable if rewritten in independent form. Claim 7 and 13 were canceled. Accordingly, Applicant believes that claims 1-6 are in condition for allowance.

Claim 9 was amended to incorporate the subject matter of claim 10, which was indicated as allowable. Claim 10 was canceled. Claim 11 was amended to depend from claim 9 and to make minor changes in the claim language to provide additional clarity. Accordingly, Applicant believes that claims 9 and 11-12 are in condition for allowance.

Claim 14 was amended to incorporate the subject matter of claim 18, which was indicated as allowable. Claim 18 was canceled. Claim 16 was amended in view of the amendment to claim 14. Accordingly, Applicant believes that claims 14, 16, 17, 19 and 20 are in condition for allowance.

Claims 26 and 31

Claim 26 stands rejected under 35 U.S.C. § 112, first and second paragraphs.

Claim 26 recites that the reset signal initializes the first region to supply the memory control signal at the first value after the power savings state. Support for claim 26 can be found on page 17, line 8 to page 18, line 4. The Office action states that reset signal 708 is not connected to and does not affect the CPU 703 or memory controller 704, only the logic at 717 and therefore the application fails to enable the claim. Applicant respectfullydisagrees. The specification, with reference to Fig. 7, states, beginning on page 17, line 30, that "[a]s computer system 701 is powered back up upon resume, power is applied, the clocks stabilize, and memory controller core 704 is initialized by RESET# such that memory controller 704 begins driving the CKE line(s) low." In an embodiment the memory controller core 704 corresponds to the claimed first region. Inherently, as one of ordinary skill would understand, the RESET# signal has to be coupled to the memory controller core 704 in order for the memory controller core 704 to be initialized by the RESET# signal. The specification clearly teaches that the reset signal 708 affects the memory controller 704. Thus, Applicant respectfully submits that the assertion in the Office action that claim language "the reset signal initializes the first region" is not enabled in the application is incorrect.

Claim 26 also recites that an asserted reset signal holds the memory control signal at the first value in the first integrated circuit during the power savings state. The Office action says "[i]t is also unclear how a reset signal, which may apparently have two states, may hold a

memory signal at a value and also initialize a circuit." Applicant points to the specification on page 17, lines 8-29, which makes clear that the RESET# signal is kept asserted during the S3 state in which the core is powered down but the I/O pad region 705 is powered Thus, during the power savings state, with RESET# asserted, the CKE signal can be kept low (asserted), and after power is reapplied to the memory controller core 704, the RESET# signal can be used to initialize the circuitry therein to drive the CKE line low. Following that period, obviously RESET# will be unasserted to allow normal operation. Thus, applicant respectfully submit that the claim is fully supported under the first paragraph of 35 U.S.C. § 112.

With respect to the term "initialize", which the Office action maintains is unclear, Applicant respectfully submits that initializing a region is well understood in the art. For example, the Modern Dictionary of Electronics, Seventh Edition Rudolph Graf, 1999 (see Appendix A attached hereto), defines initialization as a process that takes place whenever the state of a device or program must be known at startup. The specific portion of the initialization that is most relevant to the claimed subject matter is that the first region is initialized by the asserted reset signal to supply the memory control signal at the first value after the power savings state. Further evidence that initialization is an operation well understood in the art is from the primary reference Bajewa, which describes the function of reset signals in col. 6, lines 22-33. For example, Bajewa describes the PCIRST# signal as initiating the "rest of normal logic" and the CPU reset signal CPUREST# 460 is used to reset logic in the processor. As described in col. 6, lines 34-40 of Bajewa, registers are not maintained during power management mode and may contain invalid values. Bajewa teaches that the reset signals initiate the reset and initialization process for the CPU and PCI components.

Thus, Applicant submits that the language in claim 26 is clear and unambiguous, and very well understood in the art. Accordingly, Applicant respectfully requests that the rejection of claim 26 as invalid under 35 U.S.C. § 112 first and second paragraphs be reconsidered and withdrawn.

Claim 26 also stands rejected under 35 U.S.C. § 102(e) as anticipated by Bajewa. Applicant respectfully points out that there is no teaching in Baweja that the SCKE is a reset signal or that the reset signal initializes the first region. Applicant points out that Baweja teaches

reset signals (e.g., PCIRST# and CPURST#) but fails to teach either that the SCKE is a reset signal or that any of the reset signals discussed are utilized to hold the memory control signal at the first value in the first integrated circuit during the power savings state. Applicant points out that Baweja teaches in Fig. 4, that the reset signals PCIRST# and CPURST# are not even asserted while main power is off. Thus, those resets can not be used as claimed to hold the memory control signal at the first value (self refresh state) during the power savings state. Instead, Baweja teaches that the resets are used to reset the registers but there is no teaching that they are used to hold the memory control signal at the first value (self refresh state) during the power savings state. Col. 6, lines 34-35. Thus, Applicant respectfully submits that claim 26 and all claims dependent thereon distinguish over Baweja and the other references of record.

With respect to the rejection of claim 31 under 35 U.S.C. § 112, first and second paragraphs, Applicant respectfully points to the arguments made with respect to claim 26. Applicant respectfully requests that the rejection of claim 31 as invalid under 35 U.S.C. § 112 first and second paragraphs be reconsidered and withdrawn.

With respect to the art rejection of claim 31, Applicant respectfully submits that Baweja fails to teach , a reset signal that, when asserted, causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state. Claim 31 also recites recite that the memory control circuit is initialized by the asserted reset signal to supply the memory control signal at the logic level to maintain the memory in a self refresh state after power to the memory control circuit is turned on following the power savings state. Applicant submits there is no such teaching associated with the SCKE signal that the Office Action maintains is a reset signal. Thus, Applicant respectfully submits that claim 31 and all claims dependent thereon distinguish over Baweja and the other references of record.

In summary, on entry of the present amendment claims 1-6, 9, 11, 12, 14, 16, 17, 19, 20, 21, 24, 26, 27, 31-33 remain in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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APPENDIX A

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initial differential capacitance — The differential capacitance of a nonlinear capacitor when the capacitor voltage is zero.

initial drain — The current supplied at nominal voltage by a cell or battery.

initial element — *See* primary detector.

initial erection — The mode of operation of a vertical gyro in which the gyro is being erected or slaved initially. The initial erection rate is usually relatively fast.

initial failure — The first failure that occurs in use.

initial inverse voltage — Of a rectifier tube, the peak inverse anode voltage immediately following the conducting period.

initial ionizing event — Also called primary ionizing event. An ionizing event that initiates a tube count.

initialization — 1. The process in which information (memory locations for data and results, tolerances, limits, etc.) is supplied to a computer prior to the running of a program. 2. Applying input patterns to a logic circuit so that all internal memory elements achieve a known logic state. 3. A process that takes place whenever the state of a device or program must be known at startup.

initialize — 1. To set counters, switches, and addresses to their starting values at the beginning of a computer routine or at prescribed points in the routine. 2. To establish an initial condition or starting state; for example, to set logic elements in a digital circuit or the contents of a storage location to a known state so that subsequent application of digital test patterns will drive the logic elements to another known state. 3. To reset a computer and its peripherals to a starting state before beginning a task. Done automatically by the disk operating system.

initializing — 1. The preliminary steps in arranging those instructions and data in a computer memory that are not to be repeated. 2. Setting flip-flops to known states prior to testing.

initial permeability — The slope of the normal induction curve at zero magnetizing force. Permeability at a field density approaching zero.

initial program loader — The procedure that results in loading of the initial part of an operating system or other program so that the program can then proceed under its own control.

initial reversible capacitance — In a nonlinear capacitor, the reversible capacitance at a constant bias voltage of zero.

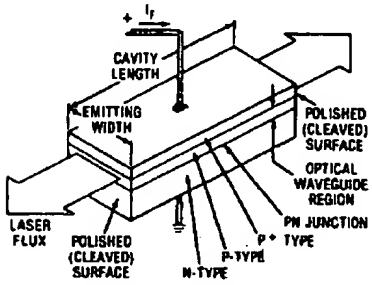
initial-velocity current — A current that flows between an electrode, such as the grid of a vacuum tube, and its cathode as a result of electrons thrown off from the cathode because of heat alone. Their velocity is sufficient to allow the electrons to reach the grid unaided by an accelerating field.

injected laser — *See* diode laser.

injection grid — A vacuum-tube grid that controls the electron stream without causing interaction between the screen and control grids. In some superheterodyne receivers, the injection grid introduces the oscillator signal into the mixer stage.

injection laser — Also known as a pn junction laser. 1. An optical oscillator or amplifier that has as its active medium a forward-biased semiconductor diode in which a population inversion has been established between the conduction and valence bands. Radiation is emitted in the process of recombination across the bandgap. High frequency modulation of the output beam can be achieved by modulating the input current. Usually, the optical resonator is formed by cleaving or polishing opposite faces of the diode crystal. Typical dimensions of the device are 0.1 mm × 0.1 mm × 0.5 mm. 2. A semiconductor diode carrying a high current in the forward direction. Radiation is produced as electrons recombine with holes in the junction region. For coherent emission, the current density must exceed a threshold commonly about 10,000 A/cm^2 for gallium arsenide diodes. 3. A solid-state semiconductor device with at least one pn junction capable of emitting coherent or stimulated radiation under specified conditions. Incorporates a resonant optical cavity. 4. A solid-state laser having at least one pn junction. Its energy level transitions are between energy bands of semiconductors and it can be tuned in frequency by temperature or pressure alterations and by the effect of a magnetic field.

injection laser diode — 1. A coherent radiant source LED consisting of an extremely flat junction area, end mirrors, and direct bandgap semiconductors, having a Fabry-Perot optical cavity. 2. In fiber optics, a semiconductor device in which lasing takes place within the pn junction. Light is emitted from the diode edge.



Injection laser diode.

injection-locked oscillator — Abbreviated ILO. A free-running microwave oscillator that is stabilized by injecting a reference signal into the oscillator's resonant circuitry. The required injected signal level is determined by the output signal characteristic requirements (i.e., noise, stability, etc.) and is typically in the range of 70 to 30 dB below the output level of the ILO.

injection luminescent diode — 1. A gallium arsenide diode, operating in either the laser or noncoherent mode, that can be used as a source of visible or near infrared light for use in triggering such devices as light-activated switches. 2. A semiconductor (gallium arsenide) diode operating in either a coherent or incoherent mode that is used as a near-infrared or visible source in triggering light-activated devices.

injector — An electrode on a spacistor.

ink — 1. One of several conductive materials used for chip bonding, electrostatic shielding, corona shielding, making connections, repairing on printed circuits, attaching leads, adhesive work, ignition cable sheath coating, and making electrodes, contacts, terminations, and surfaces receptive to plating, etc. 2. Synonymous with *composition* and *paste* when relating to screenable thick-film materials, usually consisting of glass frit, metals, metal oxide, and solvents. 3. In hybrid technology, the conductive paste used on thick-film materials to form the printed conductor pattern. Usually contains metals, metal oxide, glass frit, and solvent. 4. In thick film, composition of micrometer-size polycrystalline solids suspended in a thixotropic vehicle. The solids are chosen for their electrical characteristics (i.e., metals for conductives, metals and oxides for resistives, and glasses for glazes and dielectrics).

ink blending — *See* blending.